REMARKS

The Examiner is thanked for the thorough examination of the present application. The FINAL Office Action, however, continued to reject all claims 1-15. In response, claims 1 and 9 have been amended. Claims 2-8 and 10-15 are original. For at least the reasons set forth below, Applicant respectfully requests reconsideration and withdrawal of the rejections.

Rejections Under 35 U.S.C. 102(b) of Claims 1 and 9

Claims 1 and 9 stand rejected under 35 U.S.C. 102(b) as allegedly unpatentable by Okada et al (USPN 6,514,860 hereinafter "Okada"). Claims 1 and 9 are independent claims, from which claims 2-8 and 10-15 depend respectively. Applicant asserts that claims 1 and 9 are patentable for the reasons discussed below, and therefore for at least the same reasons claims 2-8 and 10-15 are patentable.

The examiner asserts that "Okada" discloses the method of forming a dual damascene interconnect in an integrated circuit as claims 1 and 9 recited.

Claim 1 recites:

> 1. A method of forming a dual damascene interconnect in an integrated circuit comprising:
> providing a substrate having a first etched region therein;
> filling said first etched region with a protective layer;
> coating said protective layer with a resist layer;
> ***successively patterning said resist layer and said protective layer*** to define an opening encompassing said first etched opening wherein said protective layer is recessed within said first etched opening;
> thereafter forming a second etched region encompassing a top portion of said first etched region;
> thereafter removing said resist layer and said protective layer; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

(Emphasis Added). Independent claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose at least the features emphasized above.

The method of forming a dual damascene interconnect in an integrated circuit in claim 1 comprises successively patterning the resist layer and the protective layer. Clearly, **the resist layer is patterned earlier than the protective layer.**

However, as disclosed by Okada:

> "In FIG. 3H, **a portion of the organic fill material 148 is removed** according to an aspect of the invention." (in column 9, lines 25-26 and FIG. 3H); and
>
> "Trenches 146 (best shown in FIG. 3I) are formed in the second dielectric layer 142 using conventional lithographic and etch techniques. The lithographic process involves depositing a resist 150 over the second dielectric layer 142 and exposing and **developing the resist 150 to form the desired pattern of the trenches 146.**"

(column 9, lines 50-56 and FIG. 3H)

It is clear that, in Okada's patent, **the organic fill material 148 is patterned earlier than the resist 150**. However, in claim 1, the protective layer is patterned after the resist layer is patterned. This is made expressly clear by the addition of the term "successively."

Accordingly, it is obvious that the method of forming a dual damascene interconnect in claim 1 is different from the method of forming a dual damascene interconnect in "Okada" since **the organic fill material 148 is patterned before the resist 150 is patterned**. For at least this reason, reconsideration of this rejection is hereby respectfully requested. As claim 1 defines over the cited art, dependent claims 2-8 define over the cited art for at least the same reasons.

Similarly, independent claim 9 recites:

> 9. A method of forming a dual damascene interconnect in an integrated circuit comprising:
> providing a substrate having a first etched region therein;
> filling said first etched region with a bottom antireflective coating (BARC) layer;
> coating said BARC layer with a resist layer;
> ***successively patterning said resist layer and said BARC layer*** to define an opening encompassing said first etched opening wherein said BARC layer is recessed within said first etched opening;
> thereafter forming a second etched region encompassing a top portion of said first etched region;
> thereafter removing said resist layer and said BARC layer; and
> thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

(Emphasis Added) . Independent claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose at least the features emphasized above.

It is clear that the method of forming a dual damascene interconnect in an integrated circuit in claim 9 comprises successively patterning the resist layer and the protective layer. Clearly, **the resist layer is patterned earlier than the protective layer.**

However, as noted above in connection with the discussion of claim 1, **the organic fill material 148 is patterned before the resist 150 is patterned**. Reconsideration of the rejection is hereby respectfully requested.

For at least the foregoing reasons, claims 1 and 9 are allowable over the cited reference (Okada et al). Insofar as claims 2-8 and 10-15 respectively depend from claim 1 and claim 9, these claims are also allowable at least by virtue of their dependency.

A credit card authorization is provided to cover the fee associated with the accompanying RCE application. No additional fee is believed to be due in connection with this submission. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted ,

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